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**IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-13, no. 6, December 1978, pages 799-805, IEEE, New York, US; W. STEINHAGEN et al.: "Design of integrated analog CMOS circuits - A multichannel telemetry transmitter"**

**MEASUREMENT TECHNIQUES, vol. 19, no. 9, September 1976, pages 1313,1314; D.E. POLONNIKOV et al.: "Electrometer amplifier using MOS transistors"**

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## Description

This invention relates to an amplifier circuit and, more particularly, to an amplifier circuit with a small input current which usually involves a noise problem in low frequencies of the input signal.

Examples of this type of the ordinary amplifier circuit are shown in Figs. 1 and 2. In the amplifier circuit shown in Fig. 1, N channel MOS transistors M1 and M2 form a differential amplifier. V1 and V2 designate power sources with differential terminal voltages +Vin/2 and −Vin/2, respectively. 10 designates a bias power source for the power source V1 and V2. An input signal S1 at a differential potential Vin is applied between the gates G1 and G2 of the transistors G1 and G2. Reference numeral 11 designates a current source, and Z1 and Z2 denote loads. Numeral 12 is representative of a power line connected to a high potential Vcc. GND denotes ground. The output voltage Vout of this circuit is derived from the drains of the MOS transistors M1 and M2.

In the circuit shown in Fig. 2, PNP bipolar transistor Q1 and Q2 form a differential amplifier. An input signal S1 is applied between the bases B1 and B2 of these transistors Q1 and Q2. Emitters of the transistors Q1 and Q2 are connected in series to transistors Q3 and Q4, respectively. The output voltage Vout is derived from the collectors of the transistors Q3 and Q4. A bias source 13 is provided for the transistors Q3 and Q4.

In the Fig. 1 circuit, the N channel MOS transistors M1 and M2 are used as input elements. In this type of circuit, the noise power, i.e., 1/f noise, is increased in low frequencies of the input signal. This noise originates from the physical nature of the input elements per se. The N channel MOS transistor causes noise approximately three times the P channel one. Therefore, the Fig. 1 circuit of prior art using the N channel transistor is inappropriate for use in the amplifier operating in audio frequencies.

In the Fig. 2 circuit, the PNP bipolar transistors Q1 and Q2 are used as the input elements. In this type of transistor, the base current flow inevitably and adversely influences the input signal, particularly when the input current is small. The pair of PNP transistors Q1 and Q2, and the pair of NPN transistors Q3 and Q4 are each connected in a complimentary fashion. However, it is very difficult to manufacture the transistors of the different polarities with uniform performances.

Prior art document IEEE Journal of Solid-State Circuits, vol. SC-13, No. 6, Dec. 1978, pages 799—805, discloses a voltage-to-current converter in which a pair of MOS transistors form a differential amplifier. In this converter circuit, the drains of the MOS transistors are connected to ground, and the sources of these transistors are connected to the sources of MOS transistors.

Further, prior art document Measurement Techniques, vol. 19, no. 9, Sept. 1976 pages 1313—1314, describes an electrometer amplifier in which a pair of MOS transistors which form a differential amplifier are connected with their drain terminals to the emitters of bipolar transistors.

It is an object of this invention to provide an amplifier circuit which realizes a reduction in the noise caused by the input transistor, improves the frequency response, and produces a stable output signal for a small input current applied.

To solve this object the present invention provides an amplifier circuit as stated in Claim 1.

In the present invention, P channel MOS transistors are used for the input elements. The sources of these transistors are connected to the emitters of bipolar transistors Q11 and Q12. With this arrangement, the input current is negligible, the frequency response is improved, and the noise proper to the input elements is improved.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1 and 2 are circuit diagrams of conventional amplifier circuits; and

Figs. 3 and 4 are circuit diagrams of amplifier circuits which are embodiments according to the present invention.

Reference is made of Fig. 3 illustrating a first embodiment of an amplifier circuit according to the present invention. In Fig. 3, a pair of P channel MOS transistors M11 and M12 form a differential amplifier. V21 and V22 designate differential power sources of terminal voltages +Vin/2 and −Vin/2, respectively. A junction between the power sources V21 and V22 is connected to a positive terminal of a bias power source 20. A negative terminal of the power source 20 is connected to ground GND. An input signal S1 at a potential Vin is connected between the gates G1 and G2 of the MOS transistors M11 and M12. The drains of the transistors M11 and M12 are connected to a lower potential VEE (in this embodiment, it is ground potential GND). The sources of the NPN bipolar transistors M11 and M12 are connected to the emitters of NPN bipolar transistors Q11 and Q12, respectively. The bases of the bipolar transistors Q11 and Q12 are connected together to the positive terminal of the bias power source 21. The collectors of these transistors are connected through loads 22 and 23 to a power line 24 coupled with a high potential Vcc. The potential VEE and Vcc constitute a pair of power source potentials. The negative terminal of the bias power source 21 is connected to ground GND. The output signal Vout of this circuit is derived from the collectors of the bipolar transistors Q11 and Q12.

In the above circuit, when the amplitude Vin of the input signal S1 is small, the source potentials of the MOS transistors M11 and 12 are substantially constant. The current flowing into the transistors M11 and M12 are gmVin if the voltage-current converting coefficient is gm. Then, the output voltage Vo is gmzoVin, and the voltage gain vo/vi is gmzo.

When the amplitude Vin of the input signal S1 is small, it can be considered that the voltage between the base and the emitter of each transistor Q11 and Q12 is usually constant. If the transistors M11 and M12 are operating in a saturated region, the currents M11 and M12 flowing into the transistors M11 and M12 are expressed by

$$IM1=(\beta/2)\times(VGSO+Vin/2-VTH)^2 \quad (1)$$

$$IM2=(\beta/2)\times(VGSO+Vin/2-VTH)^2 \quad (2)$$

where

$$\beta=\frac{\mu\varepsilon_{ox}\varepsilon_o W}{tox \cdot L}$$

In the above:

β: Amplification factor of the transistors M11 and M12.
μ: Mobility of hole in the transistors M11 and M12.
$\varepsilon_{ox}$: Specific inductive capacity.
$\varepsilon_o$: Inductive capacity.
tox: Thickness of the gate insulation film in each transistor M11 and M12.
W: Width of the channel of each transistor M11 and M12.
L: Length of the channel of each transistor M11 and M12.

In this case, the output voltage Vout is

$$Vout=(IM1-IM2)Zo$$

$$=\beta(VTH-VGSO)Vin=KVin \quad (3)$$

In the equation (3), VTH is the threshold voltage of each transistor M11 and M12. VGSO is a DC bias voltage between the gate and the source of each transistor M11 and M12. Further, $K=\beta(VTH-VGSO)=$constant.

The equation (3) shows that the Fig. 3 circuit can obtain an amplified output voltage proportional to the input signal.

In the circuit of Fig. 4, a bias power source circuit for biasing the NPN transistors Q11 and Q12 is composed of N channel MOS transistors M13 and M14, and a constant current source 25. The remaining circuit arrangement is the same as that of the Fig. 3 circuit. The pair of transistors M13 and M14 provide a current mirror circuit. The MOS transistor M13 is connected between the source of the MOS transistors M11 and ground. The drain of the transistor M13 is connected to the drain of the transistor M11. Its source is connected to ground GND. The constant current source 25 and the transistor M11 are connected in series between the power line 24 and ground GND. The constant current source 25 is connected to the power line 24. The transistor M14 is connected to ground. The constant current source 25 is connected at the input to the power line 24, and at the output to the drain of the transistor M14. The junction between the drain of the transistor M14 and the power source 25 is is connected to the base of the transistor Q12. The source of the transistor M14 is connected to ground GND. The gates of the MOS transistors M13 and M14 are connected together to the drain of the transistor M12. The gate of the transistor M13 is connected to its drain. The drains of the transistors M11 and M12 serve as input terminals. In the Fig. 4 circuit, unlike the Fig. 3 circuit, it is not connected to ground GND.

The bias circuit thus arranged is of the negative feedback type. In operation, when the DC level at the input is large, and a large current flows into the transistor Q11, the current mirror composed of the transistors M13 and M14 operates to decrease the base potential of the transistor Q11 and to restrict the large current. Therefore, a further stabilized operation of the amplifier circuit is ensured.

It is noted that the input elements are P channel MOS transistors M11 and M12. The 1/f noise of this type of transistor is lower than that of the P channel type MOS transistor. Therefore, if the input signal has a small amplitude and a low frequency, a lower noise is generated and therefore a high quality amplified signal can be obtained. Additionally, this type of transistor is free from the base current flow, unlike the bipolar transistor. Therefore, the adverse influence by the base current flow on the input current can be removed.

Therefore, even if the input signal is small, a stable amplified signal can be obtained.

It is further noted that, in the present invention, the source of the P channel MOS transistor M11 is connected to the emitter of the transistor Q11 or the source of the P channel MOS transistor M12 is connected to the emitter of the transistor Q12. That is to say, this circuit connection provides a cascode amplifier. Therefore, the gate-source capacitance of each transistor M11 and M12 is extremely small, and the emitter resistance of each transistor is small. The time constant, as defined by the capacitance and resistance, is small. This implies that no mirror capacitance is present, and the frequency response in high frequencies is improved, and therefore the amplifier circuit of the present invention has a good broad band characteristic. In the Fig. 4 circuit arrangement, the P channel MOS transistors and the N channel

transistors are combined. This feature provides a preferable sequence of the manufacturing steps when the CMOS-bipolar hybrid technique is used for the IC fabrication. Therefore, effective manufacturing of the amplifier circuits can be realized.

## Claims

1. An amplifier circuit comprising:
a high potential power source terminal (VCC),
a low potential power source terminal (VEE),
a pair of P channel MOS transistors (M11, M12) of which the drains are connected to said low potential power source terminal (VCC), and the gates are connected for reception of a different input signal, and
loads (22, 23), characterized in that
a pair of bipolar transistors (Q11, Q12) are connected at their emitters to the sources of said P channel MOS transistors (M11, M12);
a base bias power source (21) is connected to the bases of said bipolar transistors (Q11, Q12);
said loads (22, 23) are connected respectively to the collectors of said bipolar transistors (Q11, Q12); and
said bipolar transistors (Q11, Q12) are respectively connected through said loads (22, 23) to said high potential power source terminal (VCC).

2. An amplifier circuit according to Claim 1, characterized in that said base bias power source (1) comprises a current source (25) whose input terminal is connected to said high potential power source terminal, and a current mirror circuit (M13, M14), one input terminal of the current mirror circuit being connected to an output terminal of the current source and the bases of said bipolar transistors, the other input terminal of the current mirror circuit being connected to the drains of said MOS transistors, and output terminals of the current mirror circuit being connected to said low potential power source terminal.

3. An amplifier circuit according to Claim 2, characterized in that said current mirror circuit comprises first and second N channel MOS transistors (M13, M14), the drain of the first N channel MOS transistor being connected to the gate thereof and the drains of said first and second P channel MOS transistors, the drain of the second N channel MOS transistor being connected to the output terminal of said current source, the sources of the first and second N channel MOS transistors being connected to said low potential power source terminal, and the gates of the first and second N channel MOS transistors being interconnected.

## Patentansprüche

1. Verstärkerschaltung mit:
einem Hochpotentialspannungsquellenanschluß (VCC),
einem Niederpotentialspannungsquellenanschluß (VEE),
einem Paar von P-Kanal-MOS-Transistoren (M11, M12), von denen die Drains mit dem Niederpotentialspannungsquellenanschluß (VCC) verbunden und die Gates zum Empfang eines verschiedenen Eingangssignales angeschlossen sind, und
Lasten (22, 23), dadurch gekennzeichnet, daß
ein Paar von bipolaren Transistoren (Q11, Q12) mit ihren Emittern mit den Sources der P-Kanal-MOS-Transistoren (M11, M12) verbunden sind,
eine Basisvorspannungsquelle (21) an die Basen der bipolaren Transistoren (Q11, Q12) angeschlossen ist,
die Lasten (22, 23) jeweils mit den Kollektoren der bipolaren Transistoren (Q11, Q12) verbunden sind, und
die bipolaren Transistoren (Q11, Q12) jeweils über die Lasten (22, 23) mit dem Hochpotentialspannungsquellenanschluß (VCC) verbunden sind.

2. Verstärkerschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Basisvorspannungsquelle (1) eine Stromquelle (25), deren Eingangsanschluß mit dem Hochpotentialspannungsquellenanschluß verbunden ist, und eine Stromspiegelschaltung (M13, M14) umfaßt, wobei ein Eingangsanschluß der Stromspiegelschaltung mit einem Ausgangsanschluß der Stromquelle und den Basen der bipolaren Transistoren verbunden ist, der andere Eingangsanschluß der Stromspiegelschaltung mit den Drains der MOS-Transistoren verbunden ist und Ausgangsanschlüsse der Stromspiegelschaltung mit dem Niederpotentialspannungsquellenanschluß verbunden sind.

3. Verstärkerschaltung nach Anspruch 2, dadurch gekennzeichnet, daß die Stromspiegelschaltung erste und zweite N-Kanal-MOS-Transistoren (M13, M14) aufweist, wobei Drain des ersten N-Kanal-MOS-Transistors mit dessen Gate und den Drains der ersten und zweiten P-Kanal-MOS-Transistoren verbunden ist, Drain des zweiten N-Kanal-MOS-Transistors mit dem Ausgangsanschluß der Stromquelle verbunden ist, die Sources der ersten und zweiten N-Kanal-MOS-Transistoren mit dem Niederpotentialspannungsquellenanschluß verbunden sind und die Gate der erste und zweiten N-Kanal-MOS-Transistoren miteinander verbunden sind.

**Revendications**

1. Circuit amplificateur comprenant:
une borne de source de haute tension d'alimentation ($V_{CC}$),
une borne de source de basse tension d'alimentation ($V_{EE}$),
une paire de transistors à métal-oxyde-semiconducteur MOS à canal P (M11, M12) dont les drains sont connectés à la borne de source de basse tension ($V_{EE}$), et dont les grilles sont connectées pour la réception d'un signal d'entrée différent, et
des charges (22, 23), caractérisé en ce que
une paire de transistors bipolaires (Q11, Q12) sont connectés par leurs émetteurs aux sources des transistors MOS à canal P (M11, M12);
une source de tension de polarisation de base (21) est connectée aux bases des transistors bipolaires (Q11, Q12);
les charges (22, 23) sont respectivement connectées aux collecteurs des transistors bipolaires (Q11, Q12); et
les transistors bipolaires (Q11, Q12) sont respectivement connectés par l'intermédiaire des charges (22, 23) à la borne de source de haute tension d'alimentation ($V_{CC}$).

2. Circuit amplificateur selon la revendication 1, caractérisé en ce que la source de tension de polarisation de base (1) comprend une source de courant (25) dont une borne d'entrée est connectée à la borne de source de haute tension d'alimentation, et un circuit à miroir de courant (M13, M14), une borne d'entrée du circuit à miroir de courant étant connectée à une borne de sortie de la source de courant et aux bases des transistors bipolaires, l'autre borne d'entrée du circuit à miroir de courant étant connectée aux drains des transistors MOS, et des bornes de sortie du circuit à miroir de courant étant connectées à la borne de source de basse tension d'alimentation.

3. Circuit amplificateurs selon la revendication 2, caractérisé en ce que le circuit à miroir de courant comprend des premier et deuxième transistors MOS à canal N (M13, M14), le drain du premier transistor MOS à canal N étant connecté à sa grille et aux drains des premier et deuxième transistors MOS à canal P, le drain du deuxième transistor MOS à canal N étant connecté à la borne de sortie de la source de courant, les sources des premier et deuxième transistors MOS à canal N étant connectées à la borne de source de bases tension d'alimentation, et les grilles des premier et deuxième transistors MOS à canal N étant interconnectées.

FIG. 1

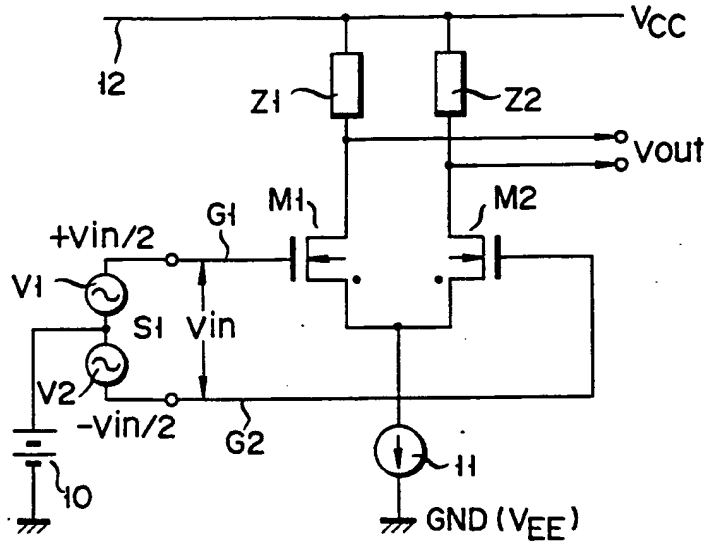

Vcc
12
Z1
Z2
Vout
M1
M2
G1
+Vin/2
V1
S1
Vin
V2
-Vin/2
G2
11
10
GND (VEE)

FIG. 2

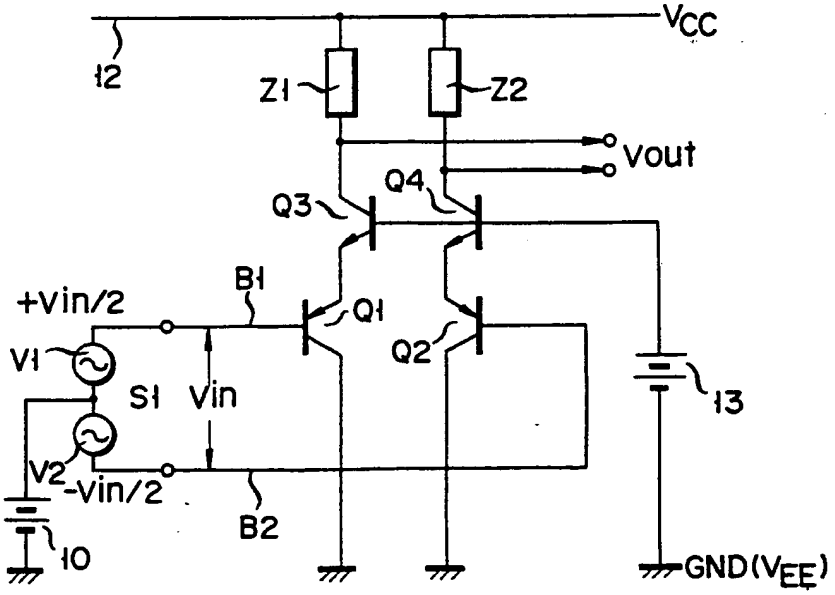

Vcc
12
Z1
Z2
Vout
Q4
Q3
B1
+Vin/2
Q1
Q2
V1
S1
Vin
13
V2
-Vin/2
B2
10
GND(VEE)

FIG. 3

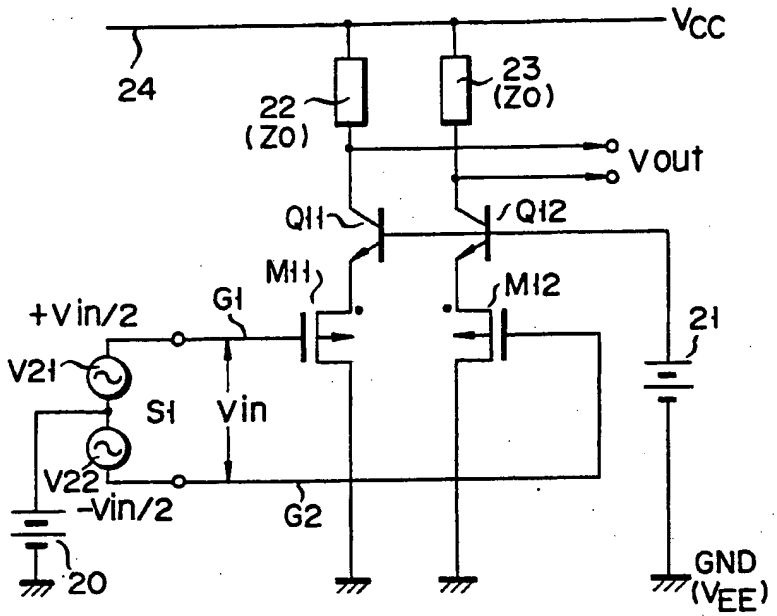
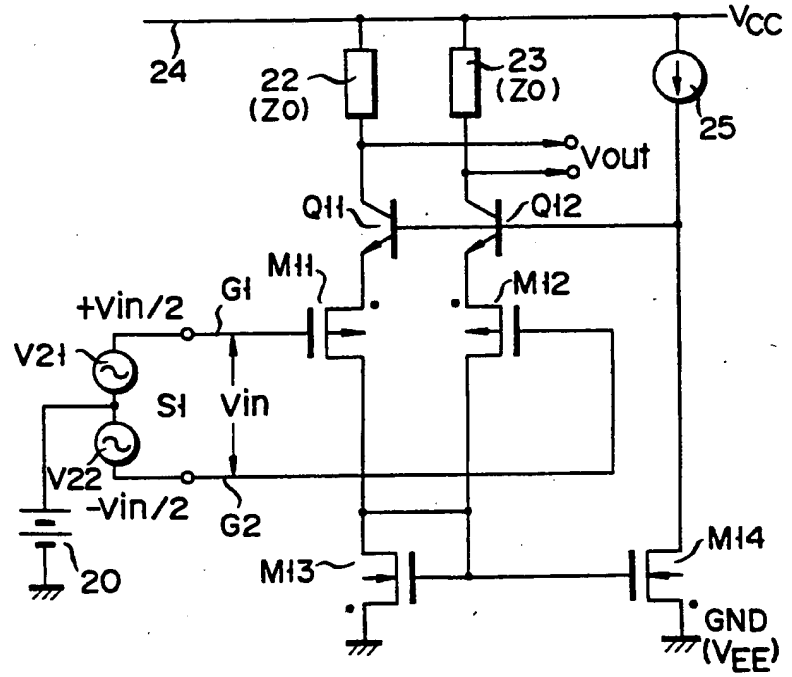

Vcc
24
22
(Zo)
23
(Zo)
Vout
Q11
Q12
M11
M12
+Vin/2
G1
21
V21
S1
Vin
V22
-Vin/2
G2
20
GND
(VEE)

FIG. 4


Vcc
24
22
(Zo)
23
(Zo)
25
Vout
Q11
Q12
M11
M12
+Vin/2
G1
V21
S1
Vin
V22
-Vin/2
G2
20
M13
M14
GND
(VEE)